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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/666,964

09/17/2003

Mahesh Anantharaman Iyer

06816.0506CON2

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7590

12/15/2005

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VANCOUVER, WA 98664

EXAMINER

HIRL, JOSEPH P

ART UNIT

PAPER NUMBER

2129

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/666,964	Applicant(s) IYER, MAHESH ANANTHARAMAN	
	Examiner Joseph P. Hirl	Art Unit 2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/03/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is in response to an AMENDMENT entered September 28, 2005 for the patent application 10/666,964 filed on September 17, 2003.
2. The First Office Action of March 30, 2005 is fully incorporated into this Final Office Action by reference.

Status of Claims

3. Claims 1-8 are pending in this application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chandra et al (IEEE 1063-8210/95, AVPGEN – A Test Generator for Architecture Verification, referred to as **Chandra**).

Claims 1, 6, 7, 8

Chandra anticipates generating a graph data structure representation, comprising one or more nodes, each node having an associated range (**Chandra**, p 190, Fig. 4); identifying a first plurality of bit-slice constraint nodes, each selecting from a range of bits of a first variable (**Chandra**, p 190, Figs. 1 and 4; Examiner' Note: ¶ 12 applies; the bit-sliced constraint nodes are the nodes of Fig. 4; the first variable is the range of bits that have been bit-sliced; bit-slice is synonymous with parsing that is well known in the industry); converting the first plurality of bit-slice constraint nodes into a second plurality of bit-slice constraints, wherein none of the bit-slice constraints, of the second plurality of bit-slice constraints, select a range of bits that overlaps with a range of bits selected by any other of the bit-slice constraints (**Chandra**, p 190, Figs. 1; Examiner's Note (EN): ¶ 12. applies; process is parsing which is generic to the industry); generating a value for the first variable that satisfies the second plurality of bit-slice constraints (**Chandra**, p 191, Fig. 6; EN: the process remains one of addition; computer implementation is addressed (Chandra, p 188, c 1:19-37).

Claim 2

Chandra anticipates the step of converting comprises: indicating, in relation to the first variable, two marking bits for each node of the first plurality of bit-slice constraint nodes (**Chandra**, p 190, Fig. 3; EN: bits related to “;” mark the node).

Claim 3

Chandra anticipates identifying a bit range, of the second plurality of bit-slice constraints, as being denoted by a first marking bit and a second marking bit, wherein a

third marking bit is not in-between the first marking bit and the second marking bit
(**Chandra**, p 190, Fig. 3; EN: bits related to “;” mark the node and a third “;” is marked
an additional set of bits.

Claim 4

Chandra anticipates selecting a value from a range determined for each bit-slice
constraint of the second plurality of bit-slice constraints (**Chandra**, p 191, Fig. 5; EN:
parsing sets the sections of the graph and the values depend on the register loading
and the process of addition).

Claim 5

Chandra anticipates concatenating each value selected from the range
determined for each bit-slice constraint of the second plurality of bit-slice constraints
(**Chandra**, p 190, Fig. 4; EN: ¶ 12. applies. Concatenating is the linking together as
represented by the graph of Fig. 4).

Response to Arguments

6. The objection to the specification is withdrawn.
7. The rejection to claims 1-6 under 35 USC 101 is withdrawn.
8. The Remarks section of the Applicant's response dated September 28, 2005 is acknowledged.

Examination Considerations

9. The claims and only the claims form the metes and bounds of the invention.

“Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)” (MPEP p 2100-8, c 2, I 45-48; p 2100-9, c 1, I 1-4). The Examiner has full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

10. Examiner’s Notes are provided with the cited references to prior art to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and spirit of compact prosecution. However, and unless otherwise stated, the Examiner’s Notes are not prior art but a link to prior art that one of ordinary skill in the art would find inherently appropriate.

11. Unless otherwise annotated, Examiner’s statements are to be interpreted in reference to that of one of ordinary skill in the art. Statements made in reference to the condition of the disclosure constitute, on the face of it, the basis and such would be

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obvious to one of ordinary skill in the art, establishing thereby an inherent prima facie statement.

12. Examiner's Opinion: ¶¶ 9-11 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense. Inclusion of the Information Disclosure Statement with the initial application would have been consistent with the spirit of compact prosecution. While the specification may contain matter that is allowable, the claims have been written in such a manner to invite a broad spectrum of prior art when ¶ 12 is applied.

Conclusion

13. Claims 1-8 are rejected.

Correspondence Information

14. Any inquiry concerning this information or related to the subject disclosure should be directed to the Primary Examiner, Joseph P. Hirl, whose telephone number is (571) 272-3685. The Examiner can be reached on Monday – Thursday from 6:00 a.m. to 4:30 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the

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Examiner's supervisor, David R. Vincent can be reached at (571) 272-3080.

Any response to this office action should be mailed to:

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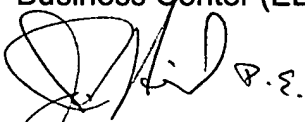
Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 273-8300 (for formal communications intended for entry.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have any questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).


Joseph P. Hirl
Primary Examiner